ST.ANNE'S
COLLEGE OF ENGINEERING AND TECHNOLOGY
ANGUCHETTYPALAYAM, PANRUTI – 607 110.

DEPARTMENT OF COMPUTER SCIENCE ENGINEERING

QUESTION BANK

EC6504-MICROPROCESSOR & MICROCONTROLLER

SEMESTER: 4 **BATCH: 2014-2018**

UNIT I
(THE 8086 MICROPROCESSOR)

1. What do you mean by Addressing modes? (May/June 2014)
The different ways that a microprocessor can access data are referred to as addressing modes.

2. What is meant by Vectored interrupt? (May/June 2014)
When the external device interrupts the processor, processor has to execute interrupt service routine for servicing the interrupt. If the internal control circuit of the processor produces a CALL to a predefined memory location which is the starting address of interrupt service routine, then that address is called Vector address and such interrupts are called vector interrupts.

3. Name the hardware interrupts of 8086. (May/June 2013, Nov/Dec 2010)
1. Divide by zero interrupt (Type 0)
2. Single step interrupt (Type 1)
3. Non Maskable interrupt (Type 2)
4. Breakpoint interrupt (Type 3)
5. Overflow interrupt (Type 4)

4. What are called as assembler directives? Give two examples. (May/June 2012)
There are some instructions in the assembly language which are not a part of processor instruction set. These instructions are instructions to the assembler, linker and loader. These are referred to as pseudo-operations or as assembler derivatives. Example: ALIGN, ASSUME.

5. What address in the interrupt vector table are used for a Type-2 interrupt in 8086?(Nov 2012)
008H (CS base address) and 00CH (IP offset) are the addresses in the interrupt vector table are used for a Type-2 interrupt in 8086.

6. Why do we use Macros? (Nov/ Dec 2012)
Macro is a group of instruction. The macro assembler generates the code in the program each time where the macro is called. Macros are defined by MACRO & ENDM directives. Creating macro is similar to creating new opcodes that can be used in the program

INIT MACRO
MOV AX,
data MO V DS
MOV ES, AX
ENDM

7. What are the general purposes registers in 8086? (Nov/Dec 2011)
AX, BX, CX, DX are the general purpose registers in 8086.

8. What is BIOS function call in 8086 μ p? (May/June 2012)
With the software interrupts you can call the desired routines from many different programs in a system.eg. BIOS in IBM PC. The IBM PC has in its ROM collection of routines, each performing some specific function such as reading character from keyboard, writing character to CRT. This collection of routines referred to as Basic Input Output System or BIOS. The BIOS routines are called with INT instructions.

9. Give the importance of the assembler directive EVEN. (Nov/Dec 2011)
The assembler derivative EVEN aligns next variable or instruction to even byte.

10. Name the registers available in 8086. (April/May 2011)
(i) General purpose registers
(ii) Segment registers
(iii) Pointers and index registers
(iv) Flag Registers.

11. What is microprocessor?
A microprocessor is a multipurpose, programmable, clock-driven, register-based electronic device that reads binary information from a storage device called memory, accepts binary data as input and processes data according to those instructions, and provides result as output

12. What is stack?
The stack is a group of memory locations in the R/W memory that is used for temporary storage of binary information during the execution of a program.

13. What is a subroutine program?
A subroutine is a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program. Thus subroutines avoid the repetition of same set of instructions in the main program.

14. What is Accumulator?
The Accumulator is an 8-bit register that is part of the arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified as register A.

15. Define instruction cycle.
It is defined as the time required to complete the execution of an instruction.

16. What are the different types of addressing modes of 8086 instruction set?
The different addressing modes are:
i. Immediate
ii. Direct
iii. Register
iv. Register indirect
v. Indexed Based indexed
vi. Relative based indexed

17. What are the different types of instructions in 8086 microprocessor?

The different types of instructions in 8086 microprocessor are:

i. Data copy / transfer instructions
ii. Arithmetic and logical instructions
iii. Branch instructions
iv. Loop instruction
v. Machine control instruction
vi.Flagmanipulationinstruction
vii. Shift and rotate instruction viii. String instruction

18. What is assembly level programming?

A program called assembler is used to convert the mnemonics of instruction and data into their equivalent object code modules. The object code modules are further converted into executable code using linker and loader programs. This type of programming is called assembly level programming.

19. What are macros?

Macros are small routines that are used to replace strings in the program. They can have parameters passed to them, which enhances the functionality of the micro itself.

20. What is the difference between the microprocessor and microcontroller?

Microprocessor does not contain RAM, ROM and I/O ports on the chip. But a microcontroller contains RAM, ROM and I/O ports and a timer all on a single chip.

21. What is linker?

A linker is a program used to join together several object files into one large object file. For large programs it is more efficient to divide the large program modules into smaller modules. Each module is individually written, tested & debugged. When all the modules work they are linked together to form a large functioning program.

22. What are procedures?

Procedures are a group of instructions stored as a separate program in memory and it is called from the main program whenever required. The type of procedure depends on where the procedures are stored in memory. If it is in the same code segment as that of the main program then it is a near procedure otherwise it is a far procedure.

23. Compare Procedure & Macro.

Procedur	Macro
Accessed by CALL & RET instruction	Accessed during assembly with name
during program execution	to macro when defined
Machine code for instruction is put only once	Machine code is generated for instruction each time when macro is called
With procedures less memory is required	With macro more memory is required
Parameters can be passed in registers, memory locations or stack	Parameters passed as part of statement which

24. **What is pipelining?**

Fetching the next instructions while the current instruction executes is called pipelining.

25. **What is a flag?**
A flag is a flipflop ,which indicates some condition produced by the execution of an instruction or controls certain operations of the EU.

26. **Draw the format of 8086 flag register.**
U U U U OF DF IF TF SF ZF U AF U PF U CF U-Undefined
CF-Carry flag PF-Parity
flag AF-Auxiliary Carry
flag ZF-Zero flag
SF-Sign flag
TF-Single step Trap flag
DF-Direction flag IF-
Interrupt enable flag OF-
Overflow flag

PART-B

1. **Explain the register Organization of 8086 processor in detail. (Nov/Dec 2010)**

The 8086 has a powerful set of registers. It includes general purpose registers, segment registers, pointers and index registers and flag register. It is also known as Programmer's model.

General purpose registers:

- The 8086 has Four 16 bit general purpose registers.
- AX , BX, CX, DX
- Each register split into two 8 bit registers
- AL – Lower byte, AH- Higher byte

Segment registers: 16 bit address

- Code segment
- Data segment
- Stack segment
- Extra segment

Pointers and index registers:

- Base pointer
- Index pointer
- Source pointer
- Source index
- Destination index

Flag Registers:

- Carry Flag
- Parity Flag
- Auxiliary Flag
- Zero Flag
- Sign Flag
- Overflow Flag

2.Draw and explain in detail about the architecture of 8086. (Nov/ Dec 2013)
8086 architecture is divided into two separate functional units
- Bus Interface Unit (BIU)
- Execution Unit (EU)

Bus Interface Unit: It Interface to the outside world. It provides 16 bit bidirectional bus and 20 it address bus.
Execution Unit: It fetches, decodes and executes the instructions. It consists of Instruction decoder, Arithmetic and Logic unit, Flag registers, General purpose registers, Pointers and index registers.

3. Explain any 8 addressing modes of 8086 processor with an example. (April/ May 2011)

Register addressing mode - MOV BX,CX
- Immediate addressing mode- MOV BL,26H
- Direct addressing mode-MOV AL,[3000H]
- Register indirect addressing mode –MOV DL, [BP]
- Base plus index addressing mode- MOV CX,[BX+DI]
- Register relative addressing mode-MOV CX [BX + 0003H]
- Base relative plus index addressing mode- MOV AL,[BX+SI+10H]
- String addressing mode- MOVS Byte.

4. Explain in detail about 8086 instruction set. (Nov/Dec 2010,2012, April/May 2011)
- Data transfer instructions
- Arithmetic and logical instructions
- Shift instructions
- Rotate instructions
- String instructions
- Program control transfer instructions
- Unconditional Jump instructions
- Iteration control instructions
- Processor control instructions
- External hardware synchronization instructions
- Interrupt instructions
- Sign Extension instructions

5. Explain in detail about Assembler derivatives and operators. (Nov/ Dec 2011,2012, April/ MAY 2011,2013)

There are some instructions in the assembly language which are not a part of processor instruction set. These instructions are instructions to the assembler, linker and loader. These are referred to as pseudo-operations or as assembler derivatives.Commonly used assembler derivatives are ALIGN, ASSUME, END, DUP, EQU, EXTRN, GROUP, LABEL, NAME, OFFSET etc.,

Variable is an identifier that is associated with the first byte of data item. In assembly language base of the number is indicated by suffix.
- B- Binary
- D-Decimal
- O-Octal
- H- Hexadecimal

6. Explain in detail about Macros. (April/May 2011)

Macro is a group of instruction. The macro assembler generates the code in the program each time where the macro is called. Macros are defined by MACRO & ENDM directives. Creating macro is similar to creating new opcodes that can be used in the program

INIT MACRO
MOV AX,
data MO V DS
MOV ES, AX
ENDM

In Macros, Parameters are passed as a part of statement which calls macros.

- Passing parameters in Macro
- Local variables in Macro
- Nested Macros
- Placing Macro definition in their own module
- Controlled Expansion statements in Macros.

7. Explain the types of interrupts and ISRSs of 8086. (Nov/ Dec 2010,2012)

Divide by zero interrupt (Type 0)

- Single step interrupt (Type 1)
- Non Maskable interrupt (Type 2)
- Breakpoint interrupt (Type 3)
- Overflow interrupt (Type 4)
- Software interrupts
- Maskable interrupts

The event that causes the interruption is called interrupt and the special routine executed to service the interrupt is called interrupt service routine.

8. Explain the interrupt structure of an 8086 microprocessor with 8086 interrupt –pointer table.(April/May 2011,2012,2014)

The event that causes the interruption is called interrupt and the special routine executed to service the interrupt is called interrupt service routine.

When the external device interrupts the processor, processor has to execute interrupt service routine for servicing the interrupt. If the internal control circuit of the processor produces a CALL to a predefined memory location which is the starting address of interrupt service routine, then that address is called Vector address and such interrupts are called vector interrupts.

In an 8086 system the first 1 Kbyte of memory from 00000H to 003FFH is reserved for storing the stating address of interrupt service routines. This block of memory is often called interrupt vector table or the interrupt pointer table.

UNIT II

THE 8086 SYSTEM BUS STRUCTURE

1.What are the advantages of Coprocessor?(May/ June 2014)

i) It is a high performance data processor.
ii) It follows IEEE floating point standard.
iii) It is multibus compatible.

2. What is meant by loosely coupled configuration? (May/ June 2014)

Loosely coupled system consists of different modules. Each module may consists of an 8086, an another processor capable of being a bus master, or processor or closely coupled configuration. Normally each processor has its own local memory and I/O devices, to which other processors do not have direct access. But they can share system resources.

3. What is the function of LOCK and RQ/ GT signals? (May/June 2013)

LOCK signal indicates that an instruction with a clock prefix is being executed and the bus is not to be used by another processor. RQ / GT signals are sampled at the rise edge of the clock pulse.

4. How does CPU differentiate the 8087 instructions from its own instructions? (May/June 2013)

8087 instructions can be distinguished from 8086 instructions by letter F which stands for floating point number. All mneumonics in 8087 begins with letter F. It has 68 instructions.

5. In what ways are the microprocessor and co-processor differ from each other? (Nov/Dec 2012 , April/May 2010)

A microprocessor is a multipurpose, programmable logic device that reads binary instructions from a storage device called memory accepts binary data as input and processes data according to those instructions and provides result as output .

The Coprocessor is a processor which is specially designed processor to work under the control of the processor and to support special processing capabilities.

6. Compare closely coupled configuration features with loosely coupled configuration features.
(May/June 2012, April/May 2010)

closely coupled configuration features:
A multiprocessor system with common Shared memory.
i) Parallelism can be implemented less efficiently.
ii) System structure is less flexible.
Loosely coupled configuration features
i) A multiprocessor system has its own Private local memory
ii) Parallelism can be implemented more efficiently.
iii) System structure is more flexible.

7. List any four 8087 data formats. (May/June 2012)
i) Word integer
ii) Short integer
iii) Short real
iv) Long real
8. What are the features of closely coupled multiprocessor systems? (Nov/Dev 2011)
i)A multiprocessor system with common Shared memory.
ii) Parallelism can be implemented less efficiently.
ii) System structure is less flexible.

9. Differentiate between minimum and maximum mode

	Minimum mode	Maximum mode
i.	A processor is in minimum mode when MN/MX pin is strapped to +5V.	A processor is in maximum mode when MN/MX is grounded.
ii.	All the control signals are given out by microprocessor chip itself.	The processor derive the status signals S2 , S1 and S0. Another chip called bus controller derives control signals using this status information.
iii.	There is a single microprocessor.	There may be more than one microprocessor.

10. What are the three groups of signals in 8086?
The 8086 signals are categorized in three groups. They are:

The signals having common functions in minimum and maximum mode.

The signals having special functions for minimum mode.

iii. The signals having special functions for maximum mode.

11. Write the advantages of loosely coupled system over tightly coupled systems

1.More number of CPUs can be added in a loosely coupled system to improve the system performance
2..The system structure is modular and hence easy to maintain and troubleshoot.
3.A fault in a single module does not lead to a complete system breakdown.

12. What is the different clock frequencies used in 80286
Various versions of 80286 are available that run on 12.5MHz, 10MHz and 8MHz clock frequencies.

13. What are the different operating modes used in 80286?
The 80286 works in two operating modes
1.Real addressing mode
2.Protected virtual address mode.

14. What are the CPU contents used in 80286?
The 80286 CPU contains almost the same set of registers, as in 8086
- Eight 16-bit general purpose register
- Four 16-bit segment registers
- Status and control register

PART-B

1.Explain Min/Max mode of 8086 microprocessor. (April/May 2011)

Minimum Mode:

- Signals connect to Vcc.
- Its is a single processor system configuration.
- The 8086, itself generate system control signal.

Minimum mode signals. eg.HLDA and HOLD

Maximum Mode:

- Signal is connected to ground
- It is a multi-processor system configuration
- External bus controller is required to generate system control signals
- Maximum mode signals. eg. LOCK

2.Describe the minimum mode 8086 system and its timing diagram.(May/June 2013)

Minimum Mode:

- Signals connect to Vcc.
- Its is a single processor system configuration.
- The 8086, itself generate system control signal.
- Minimum mode signals. eg.HLDA and HOLD

It is implemented by using two EPROMs and two RAMs. It uses driver circuit to increase the current. Timing diagram for read and write operations. The 8284 clock generator does the following functions:

- Clock generation
- RESET Synchronization
- READY synchronization
- Peripheral clock generation

3. Explain in detail about closely coupled configuration of multiprocessor configuration with suitable diagram. (April/May 2010,2011,2014)

Closely Coupled System (CCS) the processor shares clock generator, bus control logic, entire memory and I/O subsystem. Such system communicate through main memory. Data communicate in the order of bandwidth of the memory. One of the limiting factor is performance degradation which occur when two processor access the same memory. CPU is the master or host and the supporting processor is slave. The CPU provides control logic. Bus request signal from the supporting processor is connected to the CPU. In closely coupled system no special instructions like WAIT or ESC is used. Status bit is used.

4. Explain in detail about Loosely Coupled Multiprocessor configuration. (April/May 2010, Nov/Dec 2010, 2012, 2013)

- A multiprocessor system in which each processor has its own private local memory is known as loosely coupled system.
- Here the information is transferred from one processor to other by message-passing system.
- Parallelism can be implemented more efficiently.
- System structure is more flexible.

5.Discuss the schemes used to solve the bus arbitration problem in multiprocessors (Nov/ Dec 2011).

Bus Arbitration: The mechanism which decides the selection of current master to access bus is Known as bus arbitration. The three different mechanisms are commonly used are:

- Daisy Chaining
- Polling
- Independent requesting

Daisy chaining: Simple and cheaper method. All masters make use of same line for request.
Polling method: Controller is used to generate address for the masters.
Independent priority: Each master has a separate pair of bus request and bus grant lines.

UNIT III
I/O INTERFACING

1. List the features of memory mapped I/O. (April/May 2014)
(i) Maximum number of I/O devices are 1 Mbyte.
(ii) Requires decoding of 20 address lines and hence more hardware involved.

2. What are the basic modes of operation of 8255? (Nov/Dec 2013)
There are two basic modes of operation of 8255. They are:
(i) I/O mode
(ii) BSR mode

3 How to change the direction of the stepper motor from clockwise direction to anticlockwise direction using a program segment? (Nov/Dec 2012)
By reversing step sequence (excitation code sequence) it is possible to change the direction of rotation of the stepper motor..

4. Name the peripheral ICs used for parallel and serial data transfer. (April/May 2010)
8255 and 8251.

5. What are the advantages of Programmable interval Timer / Counter IC ? (April/May 2014)
(i)The 8253/8254 includes three identical 16 bit counters that can operate independently.
(ii)The 8254 is a superset of 8253.

6. What is the function of scan section in 8279 controller? (April/May 2014)
(i) Encoded scan- Scan lines are decoded externally to provide 8 scan lines.
(ii) Decoded scan- internal decoder decodes and provides 4 scan lines.

7. What is the cascaded mode of 8259 programmable interrupt controller? (April/May 2010)
The mode in which 8259s are interconnected to get multiple interrupt is called cascaded mode.

8. What is DMA? (Nov/Dec 2011, 2012)
A special control unit may be provided to enable transfer a block of data directly between an external device and memory without contiguous intervention by the CPU. This approach is called DMA (Direct Memory Access).

9. State the advantages of DMA. (Nov/Dec 2011, 2012)
(i) The data transfer is very fast.
(ii) Processor is not involved in the data transfer operation and hence it is free to execute other tasks.

10. What is the difference between two key lockout and N- key rollover modes in 8279? (Nov/Dec2010)
2-Key lock out: Simultaneous key depression is not allowed.
N-key rollover: Each key depression is treated independently from all others.

11. What is memory mapped I/O?

This is one of the techniques for interfacing I/O devices with μp. In memory mapped I/O, the I/O devices assigned and identified by 16-bit addresses. To transfer the data between MPU and I/O devices memory related instructions (such as LDA, STA etc.) and memory control signals (MEMR,MEMW) are used

12 What is USART?

It is a programmable device. Its function and specification for serial I/O can be determined by writing instructions in its internal registers. The Intel 8251A USART is a device widely used in serial I/O.

13. Write the features of 8255A.

The 8255A has 24 I/O pins that can be primarily grouped primarily in two 8-bit Parallel ports: A and B, with eight bits as port C. The 8-bits of port C can be used as two 4-bit ports:C UPPER CU and CLOWER CL.

14. What is mode 0 operation of 8255?

In this mode, ports A and B are used as two simple 8-bit I/O ports and port C as two 4-bit ports. Each port can be programmed to function as an input port or an output port. The input/ output features in mode 0 as
follows:

vii. outputs are latched
viii. inputs are not latched
ix. ports do not have handshake or interrupt capability.

15. What are the modes of operation supported by 8255?

Bit set reset mode(BSR)
I/O mode
Mode 0
Mode1
Mode2

16.Write the different types of ADC.

i. Single slope ADC
ii. Dual slope ADC
iii. Successive approximation ADC
iv. Parallel comparator type ADC
v. Counter type ADC

17. List the functions performed by 8279?

i. It has built-in hardware to provide key debounce.
ii. It provides a scanned interface to a 64 contact key matrix.
iii. It provides multiplexed display interface with blanking and inhibit options.
iv. It provides three input modes for keyboard interface.

18. What is key debounce?

The push button keys when pressed, bounces a few times, closing and opening the contacts before providing a steady reading. So reading taken during bouncing may be faulty. Therefore the microprocessor must wait until the key reach to steady state. This is known as key debounce.

19. What are the operating modes in 8279?

i. Scanned keyboard mode
ii. Scanned sensor matrix
iii. Strobed input

PART-B

1. With a neat diagram discuss the various modes of operation of 8255.(April/May 2011,2012)

There are two basic modes of operation of 8255.
They are:

- I/O mode
- BSR mode

Bit Set-Reset mode: The individual bits of Port C can be set or reset by sending out a single OUT instruction to the control register. When Port C is used for control/Status operation, this features can be used to set or reset individual bits.

I/O modes: There are three types. They are

- Mode 0 - Simple input/output
- Mode 1- Input/output with handshake
- Mode 2- Bidirectional I/O data transfer

Mode 0: Outputs are latched. Inputs are buffered. Do not have handshake.
Mode 1: input or output data transfer is controlled by handshake signals.
Mode 2: Bidirectional. Both inputs and outputs are latched.

2. Explain the parallel communication interface with microprocessor. (Nov/Dec 2012)

Interfacing 8255 to 8086 in I/O Mapped I/O Mode:

- 8086 has four special instruction in I/O Mapped I/O Mode: IN, INS, OUT,OUTS
- Only 256 address can be generated
- Only lower data bus is used as 8255 is 8 bit device
- Direct addressing mode is used.

Interfacing 8255 to 8086 in Memory Mapped I/O:

- 20 address lines to identify an I/O device
- I/O device is connected to memory register
- Address lines are used by 8255 for internal decoding
- Same control signals are used to access I/O as those of memory.

3. With neat sketch, explain the microprocessor based traffic light control system.(April/ May 2011, Nov/ Dec 2012).

The traffic light should be controlled in the following manner.

- Allow traffic from W to E and E to W transitions for 20 seconds.
- Give transition period of 5 seconds (Yellow bulbs ON)
- Allow traffic from N to S and S to N for 20 seconds
- Give transition period of 5 seconds (Yellow bulbs ON)
- Repeat the process.

Both hardware and software are used , The electrical bulbs are controlled by relays .
 I/O map is used in hardware
 Control word is used in software.

4. With the help of block diagram explain the operation of USART(8251A). (Nov/Dec 2011)
The device s which provides synchronous as well as asynchronous transmission and reception are called Universal Synchronous Asynchronous Receiver Transmitter (USART)
Features: Asynchronous protocol
 5 to 8 bit character format.
 False start detection
 Break character generation

Features: Synchronous protocol
 5 to 8 bit character format.
 Automatic sync insertion
 Baud rate from DC to 64 Kbaud.

Block diagram: It includes
 Data bus buffer
 Read/Write control logic
 Transmit buffer
 Receiver buffer
 Modem control.

5. Draw the functional block diagram of 8254 timer. (April/ May 2010,2013)
The 8254 Timer includes
 Three counters
 A Data Bus buffer
 Read/ Write control logic
 Control register
Counters: Each counter has two input signals CLOCK and GATE and one output signal OUT. It consists of a single, 16 bit, pre/settable, down counter.
Data bus buffer: Three basic functions
 Programming in various modes
 Loading the count registers
 Reading the count values.
Read/ Write Logic: It has five signals: RD , WR , CS and the address lines and .
Control Word register : It is used to write a command word which specifies the counter to be used, its mode can either read or write operation.

6. Discuss briefly about Keyboard/Display controller. (April/May 2013)
Keyboard / Display controller consists of four main sections:
 CPU interface and control section
 Scan section
 Keyboard section
 Display section
CPU interface and control section : It consists of data buffers, I/O control, Control and timing registers and control logic. Data buffers are 8 bit bidirectional buffers.
Scan section : The Scan section has a scan counter which has two modes. Encoded mode and Decoded mode.
Keyboard section: It consists of return buffers, Keyboard debounce and control, FIFO/sensor RAM and FIFO sensor RAM status. There functions depend on selected keyboard mode out of three keyboard input modes: Scanned Keyboard, Sensor matrix and Stored input.
Display section: It consists of display RAM, display address registers and display registers.

7. With a neat block diagram explain the operation of 8259 PIC. (Nov/Dec 2011)

8259 PIC includes eight blocks:

- Data bus buffer
- Read/Write logic
- Control Logic
- Three registers
- Priority resolver
- Cascaded buffer

Three registers are:

- Interrupt Request Register (IRR)

Interrupt Service Register (ISR)

- Interrupt Mask Register (IMR)

UNIT IV
MICROCONTROLLER

1. Distinguish between microprocessor and microcontroller. (April/May 2014)
Microprocessor:
(i) It has one or two bit handling instructions.
(ii) Access time for memory and I/O devices are more.

Microcontroller:
(i) It has many bit handling instructions.
(ii) Less access time for built/in memory and I/O devices.

2.List the different types of 8051 instructions. (April/May 2010)
(i) Data transfer instructions
(ii) Byte level logical instructions
(iii) Arithmetic instructions
(iv) Bit level logical instructions
(v) Rotate and Swap instructions
(vi) Jump and Call instructions

3. What are the addressing modes supported by 8051? (Nov/Dec 2010, April/May 2011)
(i) Register addressing mode
(ii) Direct Byte addressing mode
(iii) Register Indirect addressing mode
(iv) Immediate addressing mode
(v) Register Specific addressing mode
(vi) Index address addressing mode
(vii) Stack addressing mode

4. What is the difference between MOVX and MOV? (Nov/Dec 2013)
MOV: Copy the byte variable indicated by src-byte into the dest-byte location. Flags are not affected.
MOVX: Copy the contents of the external address to the accumulator, data memory etc.,

5. What are the advantages of using a microcontroller in place of a microprocessor? (May/June 2011)
(i) Flexible in design point of view.
(ii) Separate memory map for data and code.
(iii)More number of pins are multifunctioned.

6. What is the function of RET instruction in 8051? (Nov/Dec 2010)
RET pops the high and low-order bytes of the PC successively from the stack, decrementing the stack pointer by two program execution continues at the resulting address. No flags are affected.

7. What are the various operations performed by Boolean variable instructions of 8051? (April/May 2010)
(i) Logical-AND for bit variables
(ii) Logical-OR for bit variables
(iii) Move bit data.

8. Name the flags that are stored in PSW in 8051. (April/May 2011, Nov/Dec 2011)
Program Status Word is also known as Flag register. It has
(i) Carry flag
(ii) Auxiliary Carry flag
(iii) FO
(iv) Register Bank Select
(v) Overflow flag
(vi) Parity flag

9.What are the special function register?
The special function register are stack pointer, index pointer (DPL and DPH), I/O port addresses, status(PSW) and accumulator.

10. What is PSW?
Program status word (PSW) is the set of flags that contains the status information and is considered as one of the special function register

11. What is data pointer (DTPR)?
It is a 16-bit register that contains a higher byte (DPH) and lower byte (DPL) of a 16-bit external data RAM address. It is accessed as a 16-bit register or two 8-bit registers. It has been allotted two addresses in the special function register bank, for its two bytes DPH and DPL.

PART-B

1. List the features of 8051 Microcontroller. (April/May 2011,2012)
The features of 8051 are:
- 4096 bytes on-chip program memory
- 128 bytes on- chip data memory

- Four register banks
- 128 user –defined software flags
- Direct byte and bit addressability
- Binary or decimal arithmetic
- Two multiple mode, 16 bit timers/ counters
- Hardware multiple and divide in 4 microseconds.

2. Describe the architecture of 8051 with neat diagram. (Nov/ Dec 2010, April/May 2011)
8051 is a 8 bit microcontroller, It consists of
- CPU
- A and B CPU registers
- Data pointer
- Program counter
- Flag registers
- Special Function registers

CPU: It performs ALU operation
Accumulator : 8 bit register. Store the results.

Data Pointer : It holds 16 bit address.
Program Counter: 16 bit. It Holds the address of the next instruction to be executed.
Flag register: Also known as program status word

- Carry flag
- Auxiliary Carry flag
- FO
- Register Bank Select
- Overflow flag
- Parity flag

Special Function Registers: The group of registers implemented to perform special functions and are located immediately above the 128 bytes of RAM are called special function registers.

3. Explain the different types of addressing modes in 8051. (Nov/ Dec 2010, April/ May 2011) The way using which the data sources or destination addresses are specified in the instruction mnemonic for moving the data, is called addressing mode. They are

- Register addressing
- Direct Byte addressing
- Register indirect addressing
- Immediate addressing
- Register Specific addressing
- Index addressing
- Stack addressing

4. Explain the arithmetic instructions of 8051. (Nov/Dec 2010)
The arithmetic operations of 8051 include:

- Increment
- Decrement
- Addition
- Subtraction
- Multiplication
- Divison
- Decimal Operations.

UNIT V
INTERFACING MICROCONTROLLER

1. Write an ALP to receive input from port P1.5 and if it is high then an output 35H is sent to port 0. (April/May 2013)

SETB P1.5 : Configure P1.5 as an input
JNB P1.5, LAST: Skip next instruction if P1.5 is low
MOV PO, #35H: Send 35H on P0
LAST: …..

2. What are the sources of interrupt s in 8051? (Nov/ Dec 2010)

(i) External hardware interrupts 0 (INT0)
(ii) Timer 0 interrupt (TF0)
(iii) External hardware interrupts 1 (INT1)
(iv) Timer 1 interrupts (TF1)
(v) Serial Communication interrupt (RI and TI)

3. List the applications of Microcontroller. (April/ May 2008)

(i) Robotics
(ii) Embedded Systems
(iii) Automotive applications.

4. What is the function of SM2 bit in the SCON register of 8051? (Nov/Dec 2007)

SM2- Serial port Mode control bit 2.Set by software to disable reception of frames for which bit 8 is zero.

5. Define interrupt.

Interrupt is defined as request that can be refused. If not refused and when an interrupt request is acknowledged, a special set of routine or events are followed to handle the interrupt.

6. Explain synchronous data transmission.

In synchronous mode (mode 0), the instruction clock is used.
Data transfer is initiated by writing to the serial data port address.

7. What is the use of stepper motor?

A stepper motor is a device used to obtain an accurate position control of rotating shafts. A stepper motor employs rotation of its shaft in terms of steps, rather than continuous rotation as in case of AC or DC motor.

8.What is meant by key bouncing?

Microprocessor must wait until the key reach to a steady state; this is known as Key bounce.

9. What is a serial data buffer?

Serial data buffer is a special function register and it initiates serial transmission when byte is written to it and if read, it reads received serial data. It contains two independent registers internally. One of them is a transmit buffer, which is a parallel-in serial-out register. The other is a receive buffer, which is a serial-in parallel-out register

10. When are timer overflow bits set and reset?

The timer overflow bits are set when timer rolls over and reset either by the execution of an RET instruction or by software, manually clearing the bits. The bits are located in the TCON register along with timer run control (TRn) bits.

11. What are timer registers?

Timer registers are two 16-bit registers and can be accessed as their lower and upper bytes. TLO represents the lower byte of the timing register 0, while THO represents higher bytes of the timing register 0. Similarly,

TLI and THI represent lower and higher bytes of timing register 1. These registers can be accessed using the four addresses allotted to them, which lie in the special function registers address range, i.e., 801 H to FF.

12. What is the use of timing and control unit?

Timing and control unit is used to derive all the necessary timing and control signals required for the internal operation of the circuit. It also derives control signals that are required for controlling the external system bus.

13.Explain the mode (0 and1) operation of the timer.

The operations are as follows:

• Timer mode 0 and 1 operations are similar for the 13 bit (mode) or 16 bit (mode 1) counter. When the timer reaches the limits of the count, the overflow flag is set and the counter is reset back to zero.

• The modes 0 and 1 can be used to time external events.

• They can be used as specific time delays by loading them with an initial value before allowing them to execute and overflow.

14. What is meant by nesting of interrupts?

Nesting of interrupts means that interrupts are re-enabled inside an interrupt handler. If another interrupt request codes in, while the first interrupt handler is executing, processor execution will acknowledge the new interrupt and jump to its vector.

15. How is the 8051 serial port different from other micro controllers?

The 8051 serial port is a very complex peripheral and able to send data synchronously and asynchronously in a variety of different transmission modes.

PART-B

1.Discuss timers of 8051 microcontroller. (Nov/Dec2010)

- 8051 has two timers, timer 0 and timer 1.
- Both are 16 bit registers
- 8 bit microcontroller, each 16 bit register can be assessed as Low-byte register (TL)

And High –byte register (TH)

Structure of TMOD register:

- Four different modes of timer. Mode 0,Mode 1,Mode 2, Mode 3
- C/T
- Gate

Structure of TCON register:

- Start and stop timer 0and timer 1.
- Provides status of timer /Counter overflows
- Provides status of external interrupts.

2. Write a program for counter 1 in mode 2 to count the pulses and display the state of TL1 count on PORT 2. Assume that clock input is connected to T1 pin (P 3.5) (Nov/Dec 2012).

```
MOV TMOD, # 01100000B
MOV TH1, # 0
SETB P3.5
START: SETB TR1
BACK: MOV A, TL1
MOV P2, A
  JNB TF1, BACK
CLR TR1
CLR TF1
  SJMP START
```

3. Explain in detail about 8051 serial port.(April/May 2013)

- It is full duplex.
- It uses registers SBUF to hold data.
- Register SCON controls data communication.
- Register PCON controls data rate.
- SBUF is an 8-bit register dedicated for serial communication.
- Operating modes for serialport are mode0, mode 1, mode2, mode3.
- It generates baud rate in mode 0 and mode 1.

4. Explain how an LCD is interfaced with 8051. (Nov/Dec 2012, May/June 2013)

- LCD modules are available which have built in drivers for LCD and interfacing circuit to interface them to microprocessor/microcontroller system.
- LCD modules allows display of characters as well as numbers
- They are available in 16 x 2, 20 x 1, 20 x 2, 20 x 4 and 40 x 2 sizes.
- It requires less power.
- The display is organizes as two lines each of 2 characters.
- The module has 14 pins.

5.Explain the interfacing of keyboard with 8015 microcontroller. (Nov/Dec 2010, Nov/Dec 2013)

- In keyboard interfacing eight keys are individually collected to specific pins of port 1.
- Each port pin gives the status of pin .
- Logic 1 indicates that the key is open.
- Logic 0 indicates that the key is closed.
- Keyboard interface requires one input line to interface one key.
- This will increase the number of keys.
- To reduce the number of connection keys, they are arranged in matrix form.
- 16keys are arranged in 4rows and 4columns.
- It requires two ports-input and output port.
- Call debounces are allowed.